REMARKS

Applicant has amended the independent claims to add a preposition and thus make the claims more readable.

Claims 1-37 are pending in this application.

The title was objected to as being non-descriptive. Without conceding the examiner's position, the title has been amended.

Claim 37 was rejected under 35 U.S.C. § 112, second paragraph, as being indefinite. Claim 37 has been amended.

The examiner has rejected claims 1-2, 4-5, 11-12, 14-15, 21-22, 24-25, 27-28, 30-31, and 33-37 under 35 U.C.C. § 103 as being obvious over *Pereira* (U.S. Patent No. 6,697,276) in view of *Wolrich* (U.S. Patent Application Publication No. 2003/0115347).

In rejecting claims 1 and 11, the examiner stated:

> **As per claims 1 and 11, Pereira discloses allocating a memory entry in a memory device to instructions, a portion of the memory entry includes a unique identifier assigned to the instructions (col. 18, lines 36-42 and 52-60). It should be noted that computer program product in claims 1 1-20 executes the exact same functions as the methods in claims 1- 10. Therefore, any reference that teaches claims 1-10 also teaches the corresponding claims 11-20. It should also be noted that it is inherently required there be "instructions" associated with the "NFA operation" and therefore the "CAM blocks.. . enabled to participate in the NFA operation" are analogous to "memory entries allocated to instructions." Lastly, it should also be noted that the "entry type value" is analogous to the "unique identifier. "**
>
> **Pereira does not expressly disclose a multithreaded engine included in a packet processor.**
>
> **Wolrich discloses a multithreaded engine included in a packet processor (paragraph 0014, lines 2-7; paragraph 0012, lines 1-4; Fig. 2, elements 18 and 21). It should be noted that the "network processor" is analogous to the "packet processor. "**

Pereira discloses a hash CAM device that includes a memory and hash circuitry to associate a search value with a unique location within the memory. (col. 4, lines 48-50). In *Pereira*, prior to loading an entry into a storage location within the memory, the hash CAM device performs a "NFA operation" (or "next free address operation") to determine whether a hash of the entry candidate (in whole or in part) will yield a storage index to an occupied or unoccupied indexed location within the memory. (col. 5, line 58 – col. 6, line 7). In those instances in which the NFA operation indicates a conflicting occupation of the indexed location,

the hash CAM device does not store the entry candidate. (col. 6, lines 7-12). Otherwise, the entry candidate is stored at the indexed location. (col. 5, lines 24-25; col. 6, lines 12-16).

The memory of the hash CAM device may be divided into multiple hash CAM blocks. (see FIGS. 14 and 15). The examiner corresponds a "hash CAM block" of *Pereira* with "a memory entry in a memory device" of claim 1 and asserts that col. 18, lines 36-42 and 52-60 of *Pereira* discloses "allocating a memory entry in a memory device to instructions." Applicant disagrees. In the cited passages, *Pereira* discloses that each hash CAM block has a configuration register that includes an entry type value. The entry type value indicates which entry type pool the hash CAM block has been allocated to. All entries that are stored within a particular hash CAM block as a result of a NFA operation have an entry type value that is identical to the entry type value provided in the configuration register of the hash CAM block. *Pereira* may disclose allocating a CAM block to an entry type pool (e.g., an IPv4 pool, an MPLS pool, a packet classification pool, an IPv6 pool as disclosed in col. 6, lines 43-49) for use in storing entries of a particular entry type. However, an entry type pool is not an instruction. Applicant submits no portion of *Pereira* provides any disclosure of allocating a hash CAM block to instructions, much less "allocating a memory entry in a memory device to instructions," as recited in claim 1.

The examiner cites *Wolrich* solely for its disclosure of "a multithreaded engine included in a packet processor." Even if *Pereira* and *Wolrich* are combined in the manner suggested by the examiner, the combination still does not disclose all of the features of claim 1. For at least these reasons, claim 1 is allowable over *Pereira* and *Wolrich*.

Claims 11, 21, 24, and 27 contain similar limitations as claim 1 and are patentable for at least the same reasons.

> **As per claim 30, Pereira discloses a method comprising:**
>
> **allocating a content-addressable-memory (CAM) entry to a microblock, a portion of the CAM entry includes a unique identifier assigned to the microblock (col. 18, lines 36-42 and 52-60). It should be noted that the "instructions" of the "NFA operation" are analogous to the "microblock. "**
>
> **Pereira does not expressly disclose a multithreaded microengine included in a network processor.**
>
> **Wolrich discloses a multithreaded microengine included in a network processor (paragraph 0014, lines 2-7; paragraph 0012, lines 1-4; Fig. 2, elements 18 and 21).**

Assuming, for the sake of argument only, that the "'instructions' of the 'NFA operation'" of *Pereira* are analogous to the "microblock" as the examiner asserts, the examiner still has not provided any support for the position that *Pereira* discloses "allocating a content-addressable-memory (CAM) entry" to the "'instructions' of the 'NFA operation'." As previously-discussed, *Pereira* discloses allocating a CAM block to an entry type pool. An "entry type pool" is not an instruction. Applicant submits no portion of *Pereira* provides any disclosure of "allocating a content-addressable-memory (CAM) entry to a microblock" as recited in claim 30.

The examiner cites *Wolrich* solely for its disclosure of "a multithreaded engine included in a packet processor." Even if *Pereira* and *Wolrich* are combined in the manner suggested by the examiner, the combination still does not disclose all of the features of claim 30. For at least these reasons, claim 30 is allowable over *Pereira* and *Wolrich*.

All dependent claims are patentable for at least the same reasons as the claims on which they depend.

In view of the foregoing amendments and remarks, the entire application is believed to be in condition for allowance, and such action is respectfully requested.

It is believed that all of the pending claims have been addressed. However, the absence of a reply to a specific rejection, issue or comment does not signify agreement with or concession of that rejection, issue or comment. In addition, because the arguments made above may not be exhaustive, there may be reasons for patentability of any or all pending claims (or other claims) that have not been expressed. Finally, nothing in this paper should be construed as an intent to concede any issue with regard to any claim, except as specifically stated in this paper, and the amendment of any claim does not necessarily signify concession of unpatentability of the claim prior to its amendment.

Please apply any charges or credits to deposit account 06-1050.

Respectfully submitted,

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